Energy-efficient switching method using input-swapping for high-resolution successive approximation register analog-to-digital converters

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This paper presents an energy-efficient digital-to-analog converter (DAC) switching method with low common-mode variations for high-resolution successive approximation register (SAR) analog-to-digital converters (ADCs), while enabling to implement resolutions such as 14-bit as compared to the typical 10-bit. The proposed switching method enables high resolution by having a nearly constant common-mode voltage and employing input-swapping to use the reference voltage (V_{ref}) only in the sampling phase. This method eliminates the need for the third reference voltage during the entire DAC switching steps, which reduces the required number of switches at the bottom plates of the capacitors. The use of lower number of switches not only lowers the DAC control logic complexity, but also results in a faster operation, lower power, and smaller area. When compared to conventional 10-bit SAR ADCs, the proposed switching method in a 10-bit implementation reduces the average energy and area by 96.09% and 75%, respectively, while offering high-resolution implementation options such as 14 bits.

Introduction: Successive approximation register (SAR) analog-to-digital converters (ADCs) have been widely used in recent years in many applications that require low-power consumption and medium resolution such as 10-bit. There is a constant effort in literature to lower the power consumption of the SAR ADCs even further while increasing their resolutions. A large portion of the power consumption in the SAR ADCs comes from the switching power of the DACs. Recent studies in the SAR ADCs have focused on the switching power reduction of the DACs with different methods [1–7] compared to the conventional approach, but all of these methods have different drawbacks. The set-and-down switching method in [1] achieves 81.26% reduction in the average switching energy at the expense of large common-mode voltage variation that degrades the performance of the comparator, which is the main factor determining the resolution. The bi-directional switching method in [2] can provide higher resolution as it reduces the common-mode variations by using a single-side capacitor switching; however, this method consumes high reset energy, increasing the power consumption. The V_{CM}-based charge-recovery switching method in [3] eliminates the reset energy, but it needs extra voltage reference during the switching steps compared to the conventional switching method. The two-step switching method in [4] significantly reduces the power consumption; however, this method causes common-mode voltage variation, preventing its use in high-resolution SAR ADCs. The merge and split switching method in [5] sustains nearly constant common-mode voltage, while achieving great reduction in average switching energy by creating floating nodes and using two reference voltages, but this approach can lead to linearity problems, limiting its use in high-resolution SAR ADCs [6]. The proposed method in [7] needs a very small number of unit capacitors and therefore reduces the switching energy by about 99.5% compared to conventional SAR ADCs. However, this method requires V_{REFN}, V_{REFP}, and V_{CM} to perform the conversion, and again the third reference voltage can seriously degrade the resolution performance of the ADCs. Except the proposed methods in [3, 5, 7], the above methods use top plate sampling which can degrade the linearity performance due to non-linear parasitic and non-linear clock feedthrough effects. There is a need for a new switching method for achieving high-resolution and lower power SAR ADCs. This paper presents a novel switching method by using input swapping [8, 9] with bottom plate sampling and low common-mode variation. The proposed method achieves 96.09% reduction in energy and decreases the area by 75% compared to the conventional switching method used in conventional SAR ADCs with a typical 10-bit resolution, while allowing high-resolution implementations such as 14 bits.

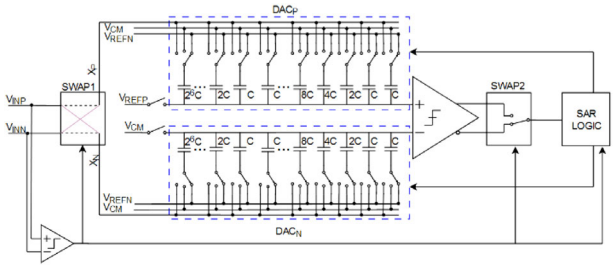

Fig. 1 *Proposed 10-bit SAR ADC architecture.*

Figure 1 shows the proposed 10-bit SAR ADC architecture, which employs two fine comparators. Before starting the actual sampling on the main DAC array, first comparison is performed by the first fine comparator to determine the polarity of the input voltage [8]. This fine comparator is only used for the first comparison. Following the first comparison, the comparator is turned OFF to reduce the power consumption. In the last five clock cycles, the comparator turns ON to implement offset calibration. As a result, the extra comparator does not lead to additional offset voltage and noise. Depending on the result of the first comparison, the DAC arrays are connected to the corresponding input voltages and actual sampling is initiated [8]. At the same time, the output of the fine comparator is also adjusted according to the output of the first comparison. At the end of the sampling, nine clock cycles are required for the conversion to determine the remaining bits. Normally, the voltage at the MSB comparison and the actual sampled voltage are different, since the input voltages are sampled in different phases. However, this limitation does not lead to an error in image sensor application, since the input voltage does not change between the first comparison and the actual sampling phase. More specifically, the outputs of the imaging sensors require certain time period for proper settling. The remaining time after sampling is sufficient for the first comparison and actual sampling of the proposed ADC. As a result, between the first comparison and the actual sampling, the input voltage remains the same. For other applications, a sample-and-hold circuit might be needed to prevent this problem.

Proposed switching method: In the conventional switching method, each of the capacitors, except the dummy capacitor, switches to either V_{REFP} or V_{REFN}, requiring large amount of switching energy. The switching energy can be reduced with the proposed method in this paper, by using either common-mode voltage V_{CM} or V_{REFN}, while V_{REFP} is only used in the sampling process. Figure 3 explains the proposed switching method for a sample 4-bit SAR ADC. For the sake of simplicity, only the case where $V_{INP} > V_{INN}$ is analyzed in the proposed switching method. The proposed method starts with the initial comparison to determine the polarity of the input voltage. During the sampling phase, V_{REF} and V_{CM} are connected to the DAC_P and DAC_N, respectively. At the end of the sampling phase, the bottom plate of the MSB capacitor, which is split into sub-capacitors [10], is connected to V_{CM}, while the bottom plates of the remaining capacitors are tied to ground in the DAC_P array. In contrast, in DAC_N, the bottom plate of the MSB capacitor is connected to ground and the bottom plates of the remaining capacitors are tied to V_{CM}. Then, second comparison is performed. If the differential input voltage is greater than V_{CM}, in the next conversion cycle, the bottom plates of the (MSB-1) capacitors are connected to V_{CM} and ground in DAC_P and DAC_N, respectively. The conversion continues until the last conversion. In the last conversion, according to the result of the previous comparison, there is no switching activity in one DAC array, resulting in a small common-mode voltage shift [11]. During the entire DAC switching, only V_{CM} and ground are used to perform the conversion. A third reference voltage called as V_{REF} is not required during the entire switching steps. As a result, the precision of the switching becomes better and does not depend on the accuracy of the third reference voltage. In the proposed architecture, the required third reference voltage V_{REF} is generated from V_{CM} voltage. Figure 2 shows the generation of the V_{REF} voltage for the sampling phase. During the first conversion phase, the V_{CM} voltage is

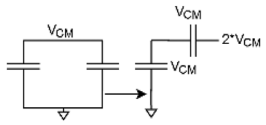

Fig. 2 *Generation of the* V_{REF} *voltage for the sampling phase.*

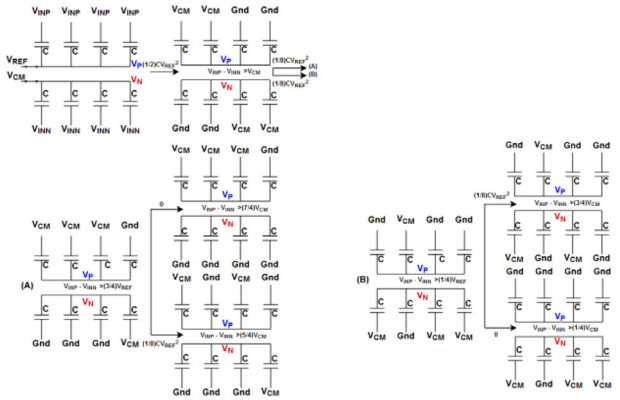

Fig. 3 *Proposed switching method for 4-bit SAR ADC when* $V_{INP} > V_{INN}$.

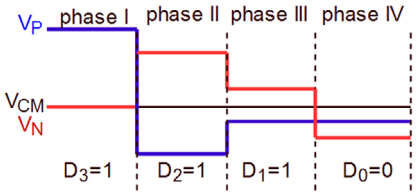

Fig. 4 *Waveform of the proposed switching method for 4-bit SAR ADC.*

sampled on two capacitors which are connected together in parallel. Following the sampling, the capacitors are connected in series to achieve a passive gain by 2 [12]. This voltage is then driven by a unity gain buffer to provide the V_{REF} voltage to the top plate of the DAC array. During the generation of the third reference voltage, from parallel to series connection, the switches lead to charge injections. In addition, the input capacitance of the input driver also causes charge sharing. However, these limitations induce only static errors, which can be corrected by using calibration algorithms.

In addition, in the proposed switching method, the parasitic capacitances coming from the layouts of the DAC arrays and switches are minimized, since the numbers of routings in the layouts are reduced by using one reference voltage during the switching. As a result, high resolution such as 14-bit can be achieved with the proposed switching method.

Figure 4 shows the waveform of the proposed switching method for 4-bit SAR ADC. In phase I, V_P and V_N are connected to V_{REF} and V_{CM}, respectively, for the sampling. The common-mode voltage has minor change in the last conversion which can be tolerable for the comparator. Therefore, the proposed scheme sustains the common-mode voltage nearly constant which provides good CMRR for the comparator while achieving good switching energy efficiency compared to the state-of-the-art methods.

In addition, for 14-bit implementation, the reduction in the energy consumption is nearly 140 pJ compared to the conventional method. The extra comparator requires 0.95 pJ/conv for 14-bit operation and it operates for six clock cycles. As a result, the 14-bit implementation of this switching method still requires less energy consumption compared to the conventional and split-cap method in [10]. 10-bit implementation of this method provides more reduction in energy consumption by using a 10-bit comparator.

DAC control logic complexity: The DAC control logic resembles to the logic used in the conventional MSB split switching method in [10], but the proposed switching scheme eliminates the MSB and (MSB-1) capacitors and reduces the number of switches during the switching. As a result, additional four switches in the proposed switching method do not increase the complexity of the DAC control logic compared to the conventional split capacitor method. Compared to the other methods without MSB split and with the third reference voltage, the number of switches increases, since in the proposed method, MSB split [10] is used. In addition, two extra signals are added in the proposed switching scheme to implement the swapping algorithm compared to the other methods. However, these additional signals do not change the complexity of the DAC array with the switches, since the DAC logic is the same during the conversion.

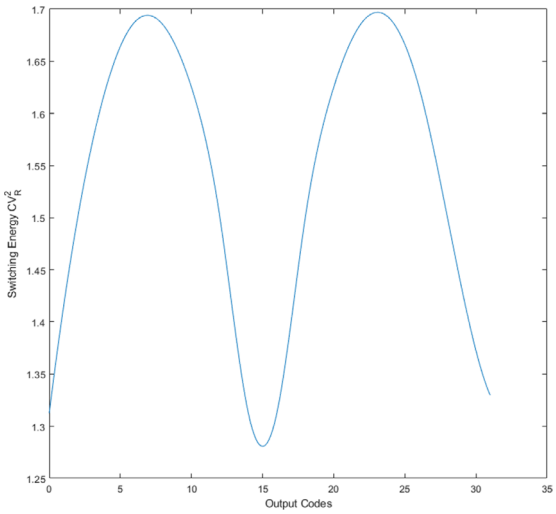

Fig. 5 *Energy consumptions versus SAR output codes for 5-bit implementation with the proposed switching method.*

Table 1. Comparison of the proposed method with published techniques for 10-bit resolution.

Switching method	Total Average Energy (CV^2)	Energy saving (%)	Area reduction (%)	Extra reference voltage	V_{CM} variation
Conventional	1363.3	0	0	No	0
Monotonic [1]	255.5	81.26	50	No	$V_{REF}/2$
Bi-directional [2]	117.05	91.4	75	Yes	$V_{REF}/4$
V_{CM}-based [3]	170.2	87.54	50	Yes	0
Split-cap [10]	851.4	37	0	No	0
CAS [13]	344.1	74.8	50	No	$V_{REF}/1024$
Tri-Level [14]	42.42	96.9	75	Yes	$V_{REF}/4$
Work in [15]	28.8	97.9	75	Yes	$V_{REF}/8$
Proposed scheme	53.33	96.09	75	No	$V_{REF}/1024$

Switching energy comparison: Figure 5 shows the energy consumptions versus SAR output codes for 5-bit implementation with the proposed switching method. The proposed scheme reduces the energy by 96.09% and area by 75% while eliminating the third reference voltage, lowering the complexity of the DAC control logic and reducing the number of switches at the bottom plate of each capacitor to implement the DAC scheme. Table 1 summarizes the results and compares the proposed scheme with the state of the art. The proposed scheme provides good energy reduction while having nearly constant common-mode voltage and eliminating the third reference voltage during the entire switching scheme.

Linearity analysis: The linearity analysis is very important for high-resolution ADCs. In the proposed SAR ADC, the worst case DNL can be seen at $\frac{1}{4}$ V_{FS} and $\frac{3}{4}$ V_{FS} where V_{FS} represents the full-scale voltage, since the MSB is determined without any capacitor division. Assume that the unit capacitor C_U has a random Gaussian distribution and a

standard deviation σ_0 [16]. The standard deviations of the maximum of INL and DNL can be written by [16]

$$INL_{MAX} = \frac{\sqrt{2^{N-2}\sigma_0^2}}{C_U} LSB \quad (1)$$

$$DNL_{MAX} = \frac{\sqrt{2^{N-1}\sigma_0^2}}{C_U} LSB \quad (2)$$

Taking the standard deviation as 1%, for 14-bit resolution, theoretically, the maximum deviations of the INL and DNL are around 0.64 LSB and 0.9 LSB, respectively. These results show that the proposed switching method is suitable for high-resolution SAR ADCs.

Conclusion: This paper proposes an energy-efficient switching method for SAR ADCs while eliminating the third reference voltage during the entire switching steps by using a technique called as input-swapping. Bottom plate sampling is used to prevent non-linearity and non-linear clock feedthrough effects. The proposed switching method achieves energy reduction by eliminating the MSB capacitors used in the conventional method, and splitting the MSB capacitor into sub-capacitor arrays. Compared to the conventional method, the proposed method reduces the energy by 96.09% in a typical 10-bit implementation. The proposed method can be easily used for high-resolution applications, like 14-bit.

Author contributions: Tayfun Akin: review and editing (equal); supervision (lead). Serhat Kocak: review and editing (equal); Original draft (lead); Conceptualization (lead); Software (lead); Formal analysis (lead)

Conflict of interest statement: The authors declare no conflict of interest.

Data availability statement: The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Received: *30 March 2023* Accepted: *1 July 2023*
doi: 10.1049/ell2.12873

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